

Power Delivery Compliance

Clock Recovery

**Pat Crowe, MQP Electronics Ltd
Sten Carlsen, MQP Electronics Ltd
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Describes possible standardized approach to recovery of clock for use in eye diagram tests

Revision History

Revision	Issue Date	Comment
0,500	December 5, 2012	Initial attempt at defining problem and proposing solution.
0,501	April 10, 2013	Proposal for final clock recovery algorithm
0,800	April 12, 2013	Modified algorithm description to specify how carrier drift and deviation drift are taken into account
0,801	April 12, 2013	Modified algorithm description to specify how carrier drift and deviation drift are compensated for.

The original of this document can be found at www.mqp.com/appnotes.htm

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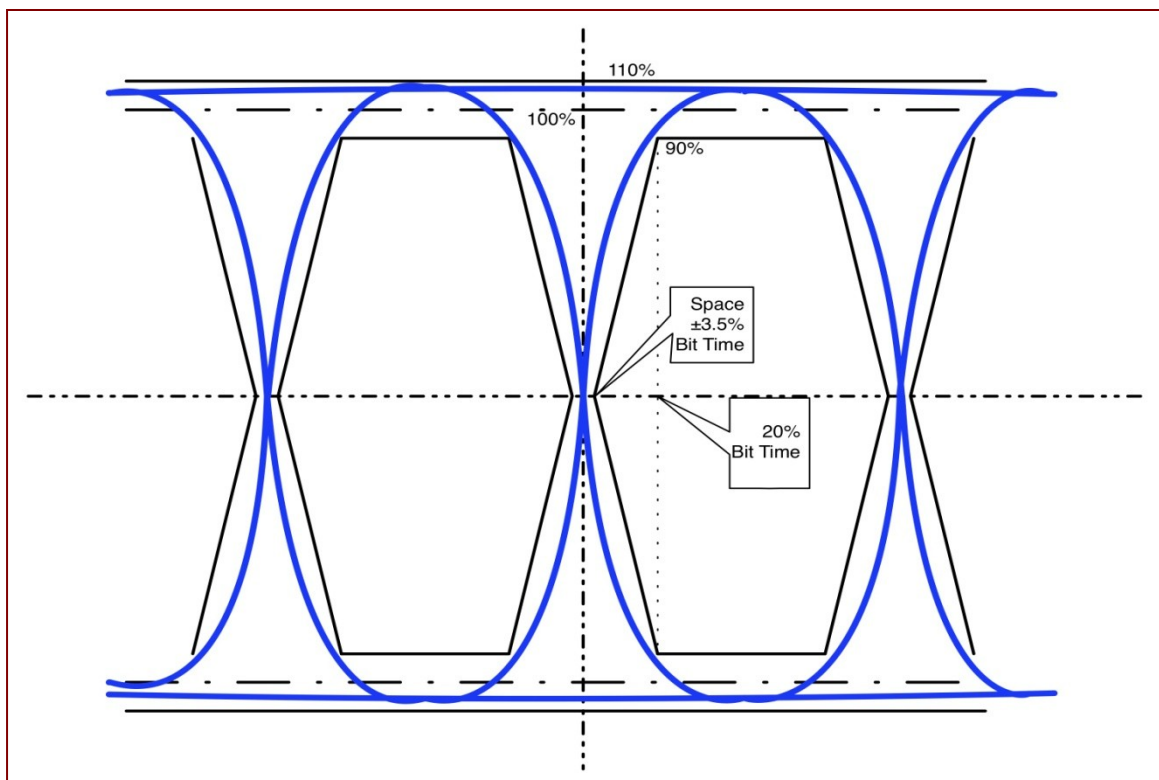
1 Eye Diagram and Bit Rate Measurement

1.1 Introduction

One of the requirements defined in the PD specification is that the transmitted data waveform shall 'fulfil the eye diagram mask in Figure 5-10' (below). The specified BIST Eye Pattern test mode outputs a continuous Pseudo-Random Bit Sequence (PRBS) and is expected to be used to demonstrate the eye diagram.

1.2 Purpose of Requirement

The purpose of the requirement is to ensure that the modulating data waveform has sufficiently low jitter at the zero-crossings, and sufficiently steep sides, to allow reliable decoding in a low-cost receiver.



Some potential problems arise when constructing an eye diagram:

- The data waveform is only available after FM demodulation of the transmitted signal.
- In order to perform eye diagram measurement the data clock is required for correct display of the waveform.
- The bit rate is allowed a certain amount of drift within a packet, so the clock period is not fixed.
- The carrier frequency and deviation are allowed a certain amount of drift within a packet, so the vertical position is potentially not fixed. It was not the intention of the original specification eye diagram to represent this drift.

Another PD compliance requirement is that the bit rate, and the bit rate drift should be measured. In practice the bit rate measurements are expected to be measured using 'BIST Carrier Mode 2', which

features a continuous signal comprising alternating 1's and 0's. Clock recovery may potentially be simpler in that case, than described below.

1.3 FM Demodulation

In principle, a typical PD receiver will implement an FSK demodulator, which by its nature will have square edges. To be able to display the transmitted data waveform, we will need to implement an FM demodulator, which attempts to recover the waveform as faithfully as possible. In order that different vendors do not produce test equipment which gives different results, it may be necessary to define certain aspects of this FM demodulator.

1.4 Clock Recovery

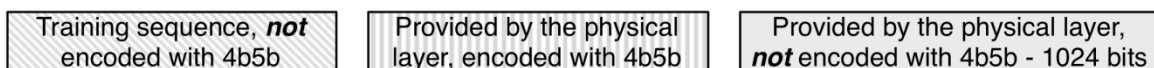
In an ideal situation the clock used for the display of the eye diagram would originate at the transmitter (in the Unit under Test, or UUT) and would be connected directly to the eye diagram display equipment. However it is a characteristic of the PD UUT that this signal is not available, and that all tests take place on the accessible VBUS connection which passes between units.

Therefore we need to use a clock recovered from the data after demodulation. The algorithm used for clock recovery must be defined so that test equipment from different vendors generates an equivalent recovered clock.

The eye diagram should be constructed, and the bit rates measured, using data runs equivalent to the longest packet used in PD, which is the packet sent in the BIST Transmit Mode.



LEGEND:



This has a total of $64 + 20 + 1024 = 1108$ bits. Note that the BIST Eye Pattern test mode transmission uses the same PRBS but does not contain a preamble.

1.4.1 Reference Frequency

For each packet transmitted the PD specification defines the reference bit rate to be the average bit rate of the last 32 bits of the preamble. This is the bit rate against which any bit rate drift is measured.

1.4.2 Clock and Bit Rate Recovery Algorithms

As the bit rate is allowed to drift by up to 0.25%, this could result in an error after 1044 bits that could amount to 2.61 bits, given worst case distribution of the drift. It is clear that either the recovered clock frequency, or its phase, must vary over the equivalent packet length.

If the frequency is required to vary from the reference frequency, then the main question would be the loop bandwidth of the clock recovery function. A narrow loop bandwidth would tend to result in the bit error described above, and a wide loop bandwidth could result in the recovered clock exactly corresponding to the zero crossings. Neither method provides meaningful measurements.

Alternatively we can adopt a method of recovery which takes the reference clock frequency as its basis, and adjusts the phase to align with the zero crossings.

It is intended that the technique used be a reasonable model of what a practical receiver may achieve in a real-time environment. The method described below employs the reference frequency, but regularly adjusts the clock phase to allow a symmetrical eye diagram representation. **It compensates continuously for the carrier drift, though not for the deviation drift.** This is considered to be a reasonable and repeatable representation of how a low-cost receiver may perform.

Measurements of f_{Carrier} , $f_{\text{Deviation}}$, $p_{\text{CarrierFreq}}$, p_{DevFreq} , p_{BitRate} and f_{BitRate} are made separately in other PHY chapter tests.

Reference Bit Rate measurement algorithm

The proposed method of determining the reference bit rate is as follows:

- Choose a sequence of 32 bits starting at a zero crossing (if these bits do not end in a zero crossing take as many more bits as are needed to end on a zero crossing).
- Fit a fixed rate clock to these bits, using a least mean squares technique on the zero crossing errors over this number of bits.
- This defines the reference bit rate of the recovered clock at the start of the following 1044 bits.

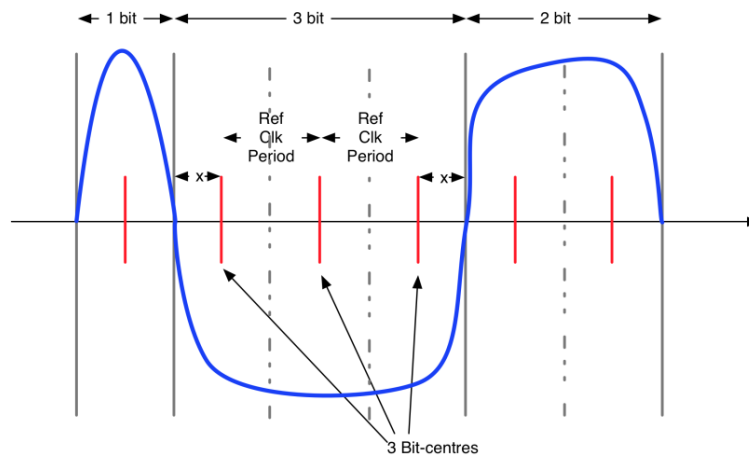
Continuous Carrier Frequency measurement algorithm

During the 32 to 39 bits mentioned above and during the next 1044 bits, a running measurement is made of the carrier frequency, in order to determine the zero-crossing y-value. The data waveform is examined at a point 1.5 bit periods after the most recent zero-crossing, thus allowing the signal to settle. Each time a new reading is taken, the assumed carrier frequency is calculated as being half way between the current reading and the previous one of opposite polarity.

Clock recovery algorithm

The proposed method of recovering the clock is as follows:

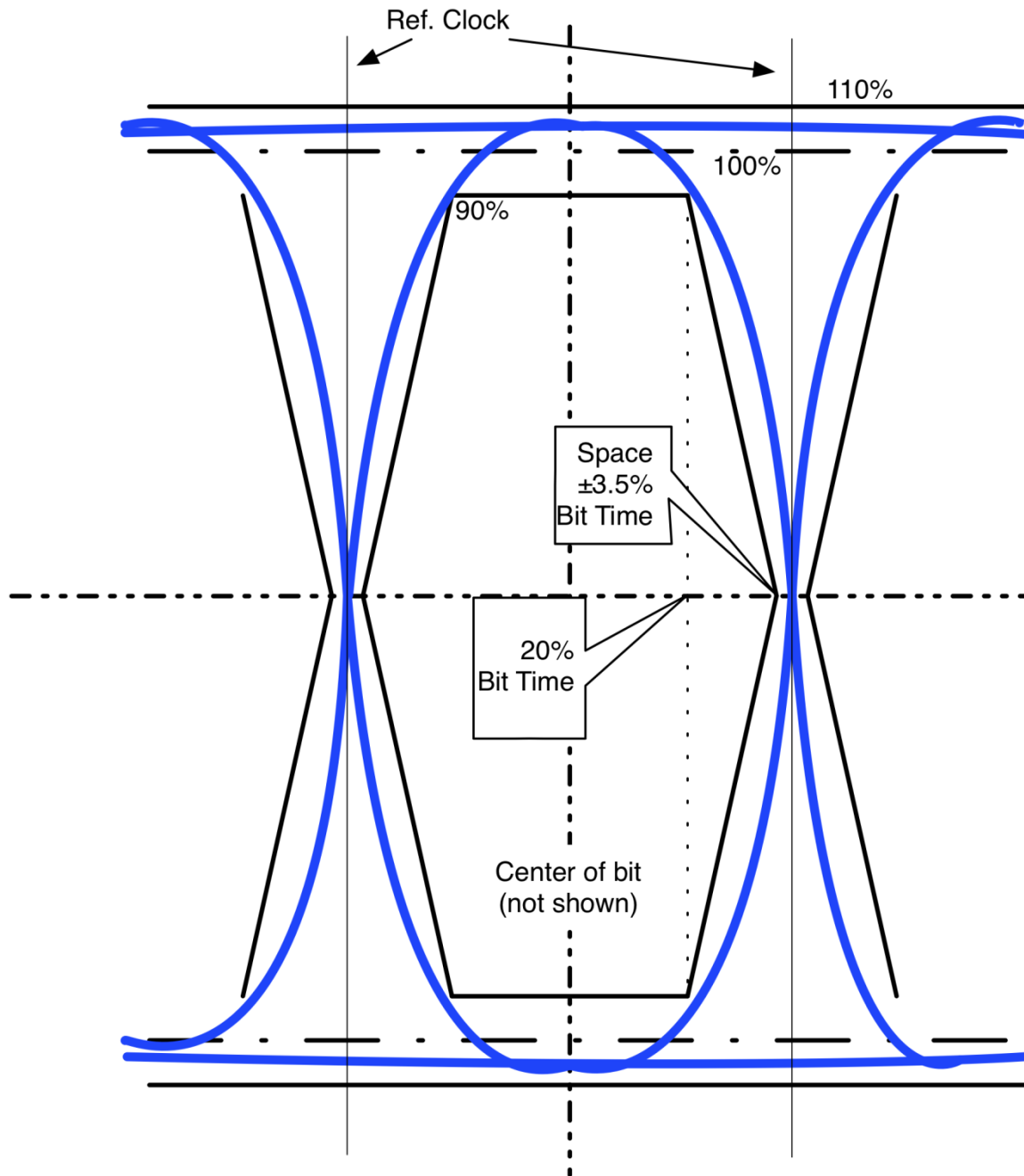
- Assume the x-axis of the eye diagram to be the most recently calculated Carrier Frequency value, and that a zero-crossing is defined as the time at which the demodulated data signal crosses this line.
- Note the position (in time) of each zero-crossing pair.
- Using the value of the reference clock rate, calculate the number of bits between these two zero-crossings (n).
- Insert n notional bit centre positions, each spaced apart at the reference clock period, and placed symmetrically between the two zero-crossings, so that the two distances marked x are the same.
- Plot the data waveform around each bit centre position onto the eye diagram.



Eye Diagram

(See figure below)

The eye diagram display is logically centered around the recovered bit centre positions, so that a single bit occupies the centre of the diagram. The bit-centers identified in the clock recovery algorithm are positioned in the centre of the diagram, and the diagram then accurately reflects the jitter of the zero-crossings, and the steepness of the 0->1 and 1->0 transitions.



The worst possible case for the effect of the 0.25% max bit rate drift is that, in the case of a run of 8 bits of the same value, the change in frequency would contribute 4 bits \times 0.25% = 1% displacement of the clock edge, out of a budget of 3.5%

Using this method of plotting appears to give a good overall representation of the signal quality.