Application Note 30701

In-System Programming of EPCS1/4

This application note describes how EPCS1/4 Serial Configuration Devices may be programmed in-circuit using the dedicated JTAG/ISP connector on the Pin-Master 48 universal programmer. The programming cable, the design of the target board, and programming procedures are described.

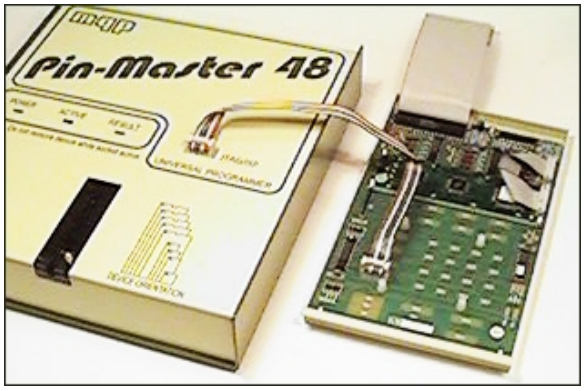
INTRODUCTION

EPCS1/4 are 1 and 4 Mbit flash memory devices used to serially configure Altera Cyclone FPGAs. With proper attention to circuit design they can be serially programmed while in the end-users target system.

In system programming reduces the number of times the parts have to be handled during the manufacturing process and allows the latest or custom logic patterns to be loaded just prior to shipping.

As a result of the short programming time, the use of a single site programmer with a dedicated ISP connector on a production line becomes an attractive and low-cost alternative to a separate gang programming operation.

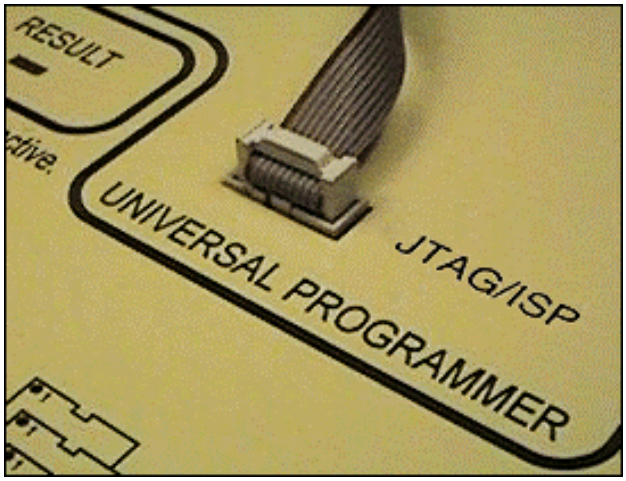
The serial interface between the programmer and target board is made up of four lines for clock,data and chip select, and two lines for power and ground.



Production Programming using Pin-Master 48

The Pin-Master 48 universal programmer has a dedicated JTAG/ISP connector fitted to the top of the unit. A cable made up to the users own requirements connects the socket to the target board.

The requirements of in-system programming affects the circuit design of the target board. Aspects of the design which must be considered are explained in detail later in this application note.



JTAG/ISP SOCKET

The socket is a standard 10 way 0.1″ header. A diagram of the socket is shown below:

Viewed from top, front of programmer

2 GND	4 GND	6 GND	8 GND	10 GND
1 nCS	3 VCC (nCE)	5 ASDI	7 DCLK	9 DATA

1	nCS	EPCS4 Chip Select
2	GND	Ground
3	VCC	Voltage Supply
4	GND	Ground
5	ASDI	Data to EPCS4
6	GND	Ground
7	DCLK	Clock to EPCS4
8	GND	Ground
9	DATA	Data from EPCS4
10	GND	Ground

CABLE

A ribbon cable with alternate wires connected to ground is used between the Pin-Master 48 and the target board. The cable should be kept as short as possible (maximum length 1.5m).

TARGET BOARD

CONNECTOR

The target board should be equipped with a suitable connector. This could be most simply achieved with a similar connector and pin layout to that used at the programmer end of the cable.

- ***GND Pins 2, 4, 6, 8 and 10***

Connect these five pins to the target system ground.

- ***DCLK***

Pin 7 of the ISP connector must be connected to the clock pin (DCLK) of the device. Any other circuit connected to DCLK for normal operation must be high impedance when in the programming mode. This ensures that the logic level margins are maintained. When the EPCS1/4 is being used with a Cyclone FPGA this may be achieved by a holding the nCE pin of the Cyclone device to VCC. A suitable source of VCC may be the VCC connection from the Pin-Master 48 ISP socket.

Note: Most problems with in-system programming are caused by spurious clock signals due to crosstalk. Steps should be taken to prevent such problems; a suggested solution is shown in the following diagram.

- ***ASDI***

Pin 5 of the ISP connector must be connected to the data in pin (ASDI) of the device. Any other circuit connected to ASDI for normal operation must be high impedance when in the programming mode. (see comments under DCLK above).

- ***nCS***

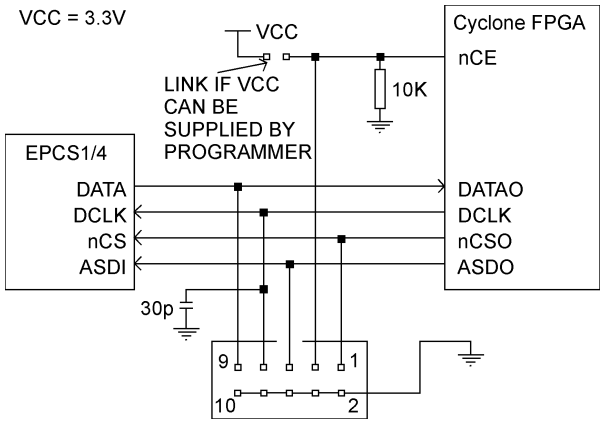
Pin 1 of the ISP connector must be connected to the chip select pin (nCS) of the device. Any other circuit connected to nCS for normal operation must be high impedance when in the programming mode. (see comments under DCLK above).

- ***VCC***

The VCC pin of the ISP connector may be directly connected to the VCC pin of the device. This is only possible if the circuit requires less current than the Pin-Master 48 can supply.

The maximum current that should be drawn from the programmer is 150mA at +3.3V. The

maximum capacitance allowed on the VCC line is 10µF.



Typical Target Board Circuit Arrangement

The target board may be completely powered from the programmer if its total requirements do not exceed those specified above.

In the event that the programmer VCC cannot be used to power the target board then the cable VCC connection could be left unconnected, and the target board powered by a separate PSU.

As explained above the VCC signal offers a useful way to apply a high level to the cyclone FPGA to prevent it driving the three inputs DCLK, nCS and ASDI of the EPCS1/4. This signal is high during programming only. Other arrangements are possible where the programming cable connector is used to route the target board's own VCC to the nCS pin.

PROGRAMMING PROCEDURE

To avoid earth potential differences, if the target board is powered separately, the programmer and target board should be connected to a common mains supply.

- Connect the cable to the target board and the programmer.
- Power up the target board, if necessary, and proceed with programming in the normal way.
- If there are any other devices to be programmed on the board move the cable and repeat the procedure. This could be simplified by using a 'Script' (batch file) which would automatically change the device type and instruct the operator where to plug in the cable.

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