Packet-Master PDT-EPR Power Delivery Compliance Tester

*The **Packet-Master PDT-EPR** is a USB Power Delivery Compliance Tester and development tool. It is based on our extremely successful USB-PDT model but has been enhanced to address the new requirements of EPR (Extended Power Range).*

*The PDT-EPR comes complete with our Windows application **GraphicUSB** for driving and reporting on the Compliance Tests and capturing and displaying every detail of the PD interactions.*

The Packet-Master PDT-EPR from MQP is the world's first comprehensive Power Delivery Compliance Tester, for testing protocol, measuring signal quality and power load testing, all within one compact unit.

Power Delivery

Power Delivery is a specification allowing USB to provide power in a more flexible and adaptable way. It uses two-way signalling on the CC wire of a USB C-cable.

Power Delivery Compliance Tester

The Packet-Master PDT-EPR behaves as one end of a PD link. It can emulate the behaviour of an initial Source or Sink in controlled ways, and as such is able to confirm the responses of the connected Unit Under Test (UUT).

Cable Marker Compliance Tester

It is also designed to perform all the required protocol and PHY Compliance Tests on Electronic Cable Markers. Nothing extra is required for these tests.

Analyser

Analyser functionality is always available. An additional Analyser Pod is required to allow analysis of PD between two external PD devices.

Background

PDT-EPR has been designed in conjunction with the USB-IF PD CTS Compliance Specification. Virtually any non-compliance with the protocol, timings, signal quality, or power control will be revealed, and a detailed description of the problem displayed.

Resources

The Tester is built around a 250Ms/s ADC and DAC, plus a number of other critical resources (see Table on next page)

Software/firmware updates are generally available free of charge from our website.

Report and Analysis Operation

The Packet-Master PDT-EPR detects and displays the following in a simple-to-understand yet informative manner:

- Every PD message packet, including full detail of the preamble bits, SOP ordered set, header and data objects. Every bit field is analysed, described and any potential non-compliances are highlighted.
- Bit Stream and other continuous waveforms are displayed, with an analysis of their type.
- The VBUS voltage and current are monitored and displayed, on a zoomable timeline which also shows the CC line state and actual PD message packets. Discrepancies between voltage and current changes and the occurrence of related messages are clearly shown.
- SOP', SOP'', SOP'_debug and SOP''_debug messages are also displayed.

In minimum display mode, the graphical display shows Atomic Message Sequence (AMS) headers, allowing a quick overview summary of the significant PD events. While in that mode, these headers can be double-clicked to reveal every PD packet in that segment of the event display.

Plug-In Modules

A special feature of the Packet-Master PDT-EPR is the use of a plug-in module for the connections to the Unit Under Test.

This has the advantage that changes to the official test requirements do not necessarily require complete replacement of the PDT Tester. The original BT2 Plug-in has now been replaced by the BT3 Plug-in. This resulted from new test requirements relating to PD Revision 3.

The most vulnerable connector on the Plug-in is the Type-C receptacle. This is a user replacable part.

Requirements

The minimum requirements for the Packet-Master USB-PDA Host are as follows:

- x86/x64 Architecture
- High Speed USB 2.0 port or better dedicated to the PDT-EPR.
- Windows 7 up to Windows 11.
- 4GB RAM
- 10GB space on Hard Disk

Tester Resources

The tester has a number of built-in resources which contribute towards its capability as a comprehensive PD Compliance Tester: In general these resources are under the automatic control of the software, so for example capturing an Eye Diagram results from starting one particular test.

Signal Receiver	A 250Ms/s ADC samples the incoming signal. This is fed to programmable logic capable of filtering the signal, and also of storing the captured samples in order to perform Eye Diagram analysis on them. The Eye Diagram is plotted using the algorithm specified in the CTS Compliance Test
Signal Transmitter	The outgoing signal is generated by programmable logic, feeding a 250Ms/s DAC. This allows the generation of any shape of transmitted signal, from perfect signals to signals with any degree of simulated interference. Signals may of course be generated at any bitrate. The offset is also controllable. A Bus Idle condition with programmed agression signal and programmed offset can also be generated.
Power Delivery Protocol Engine	A fully compliant policy/protocol engine emulates the behaviour of an ideal device, or deliberate errors may be introduced. As this is based on downloadable logic the engine specification can be kept up to date by means of software downloads, generally available free of charge from our web site.
Power Delivery Analyser	A non-intrusive PD Analyser provides captures of every detail of the PD protocol and timing between events. The analysis includes a zoomable time-line, which also displays VBUS voltage and current waveforms, allowing a quick check on message versus power timings.
VBUS Voltage Measuring Circuit	Measures VBUS voltage at up to 1Ms/s. 0V to +55V
VBUS Current Measuring Circuit	Measures VBUS current at up to 1Ms/s. 0V to +10A
Full Programmable PD Engine	Implements standard/programmable PD Policy Manager, Policy Engine and Protocol Engine, together with Cable Marker emulator.
VBUS Generator Circuit (240W)	Generates VBUS from 0V to 48V at up to 5A in steps of 1mV. Has programmable current to allow PPS current limit mode.Designed to meet PD specifications.
VBUS Programmable Current Load (240W)	Sinks currents up to 5A in steps of 10mA, or power up to 240W in steps of 250mW, with programmable rise and fall times. Designed to meet PD specifications.

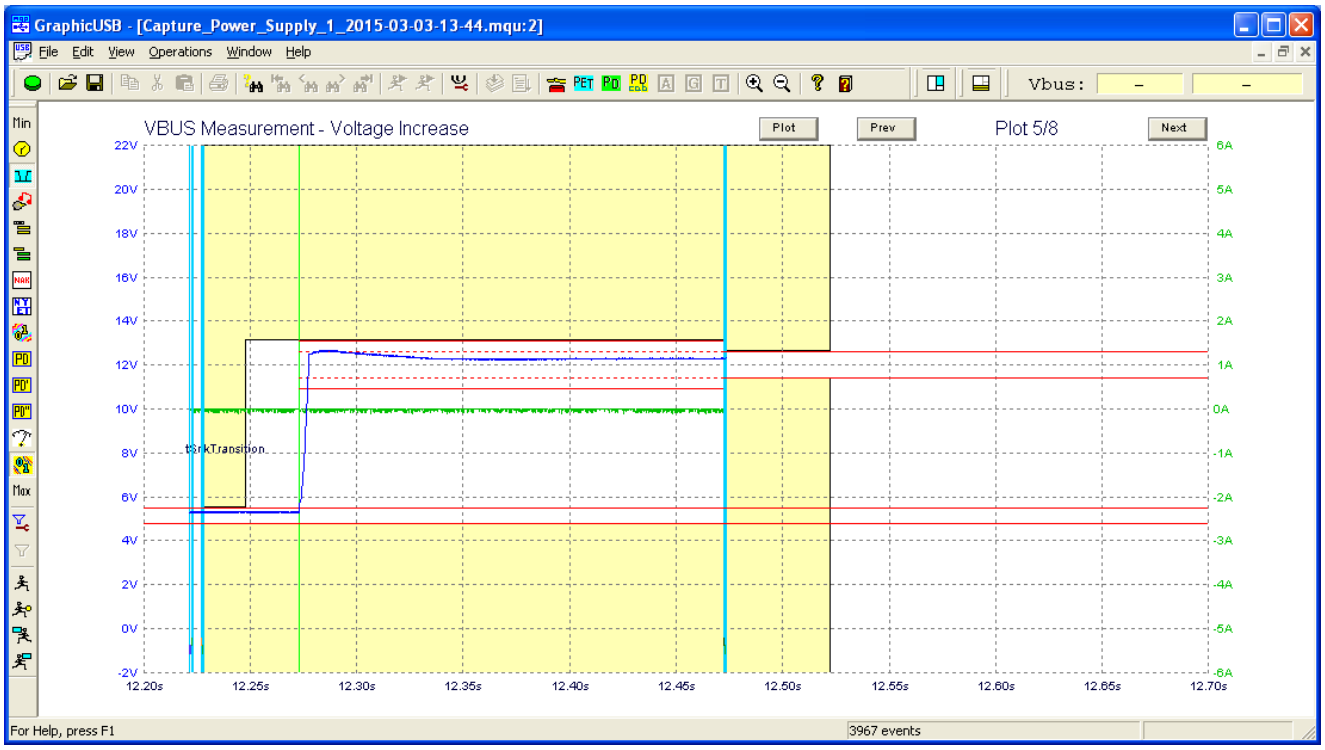
PDT-BT3-CON Plug-in Module Resources

Revised Specification Noise Generator	The BT3 plug-in features a noise generator meeting the new requirements of the Compliance Workgroup. Both two-tone and Arbitrary Waveform Generator methods are user selectable, as well as the classic square wave method. This allows full certainty whether the UUT complies with the interference rejection requirements of the PD Specification, as some other test equipment vendors only implement one of these methods.
Fully Implemented Type-C State Machine	The BT3 plug-in features an FPGA with accurate fully-implemented Type-C State machine. The actual Type-C states are reported back to the capture file for better understanding of the functioning of the UUT. This will allow all Type-C devices to be tested in the future.
Special Test Cable with both CC1 and CC2 End to End.	The Special Test Cable provided has both CC1 and CC2 lines connected end to end. It is a 5A cable with no cable marker. It is specially calibrated to allow voltage measurements at the remote end of the cable. • Allows the Tester to choose to assert Ra at remote end of test cable. • Allows the Tester to detect and measure VCONN at remote end of test cable. VCONN can also be measured under load using the VCONN Current Sink. • Allows the Tester to perform tests with flipped connector without user intervention.
Fully adjustable VCONN Generator	VCONN can be set to any value from 2.75V up to 5.75V. Among other things, this allows the cable marker test to run automatically at a selection of VCONN voltages as required by the test plan.
Adustable VCONN Current Sink	This can be used to check the capabilities of the remote VCONN supply.
VCONN input and output Current Measurement	This can be used to check the VCONN current drawn by the UUT.
Voltage Measurement on CC1 and CC2	Precision measurements on CC1 and CC2 are made at 8µs intervals. This allows the PDT to take 'scope' captures of VCONN and CC voltages, with a future SW upgrade.
Dual FRS Test Outputs	In conjunction with our PDT-FRS Mains Switching unit, and similar vendor supplied units, this allows the FR_Swap tests to be automated.
Scope Trigger Output	This can be programmed to provide a scope trigger output on seeing any PD message specified, or other available events. Very useful during development, and project debugging.
Buffered CC1 and CC2 Scope Outputs	If required, an oscillosope may be connected to the outputs without fear of altering the voltages on the CC lines.
Indicators	Front panel indicators are provided for Vbus=5V, 3V > VBUS > 5V, VBUS > 5V, Rp active, Rd active, Ra active, CC1 is data, CC1 is VCONN, CC2 is data,

	CC2 is VCONN, FPGA loading, FPGA erasing, FPGA Flash programming, plus spare indicators for future use with upgrades.
Type-C Connector for UUT	The Plug-in is fitted with a user-replacable Type-C connector to simplify problems caused by normal connector wear and tear.
Calibration Connectors	A separately available Calibration Jig may be connected to special calibration connectors on the front panel. This allows the PDT and Plug-in to be user-calibrated without returning to the manufacturer.
High Speed Communication Channel with Motherboard	The BT3 plug-in communicates with the PDT unit via a 10MHz communication channel. This guarantees much more accurate reporting on bus conditions.
BC 1.2 Functionality	The BT3 plug-in automatically checks whether BC 1.2 has been implemented on the UUT, and will report this in the capture display.
Fully Programmable Rp Current Source, plus resistive Rp	Rp is implemented with a fully programmable circuit allowing marginal test conditions to be applied if required.
Rd and Ra resistors	In addition to nominal values for Rd and Ra, the tester also allows all min and max values allowing marginal test conditions to be applied if required.

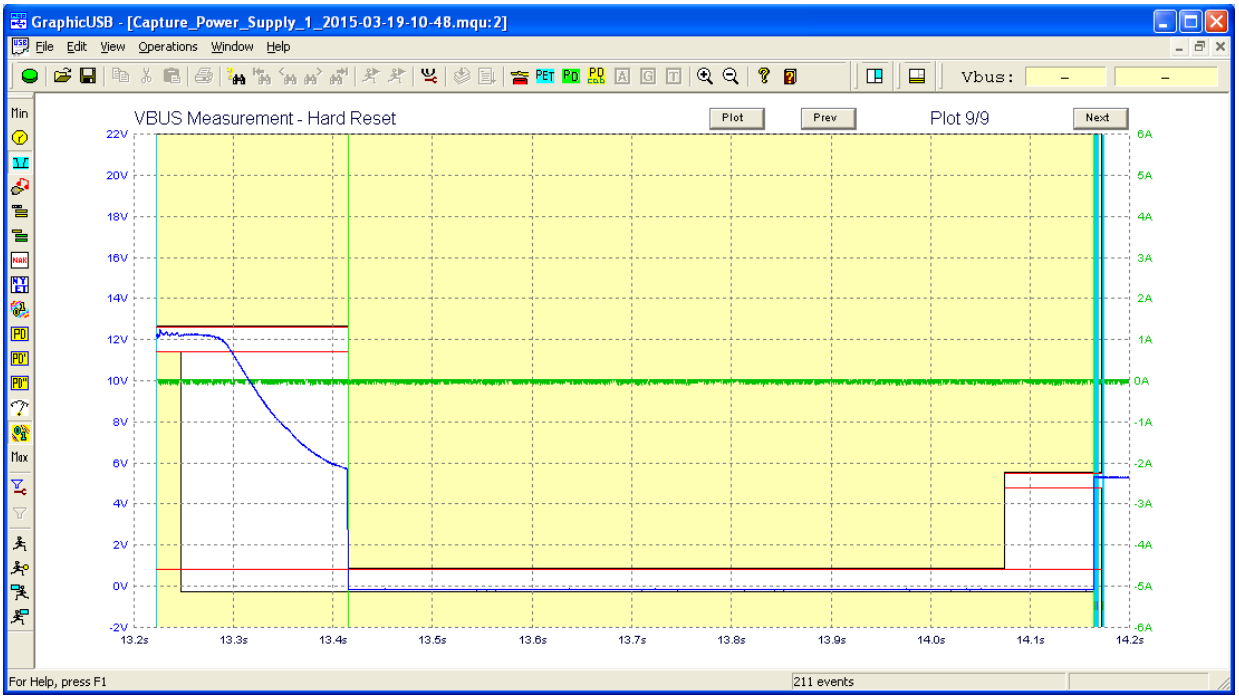
Voltage/Current Scope Captures

During a Compliance test involving a Transition, the VBUS voltage and current waveforms are captured, and plotted against the appropriate mask. The example above shows a positive voltage transition. The blue vertical lines show the boundaries of the PD messages (described in more detail on zooming in, see example on following page). The waveforms would be coloured red where they intersect the mask.

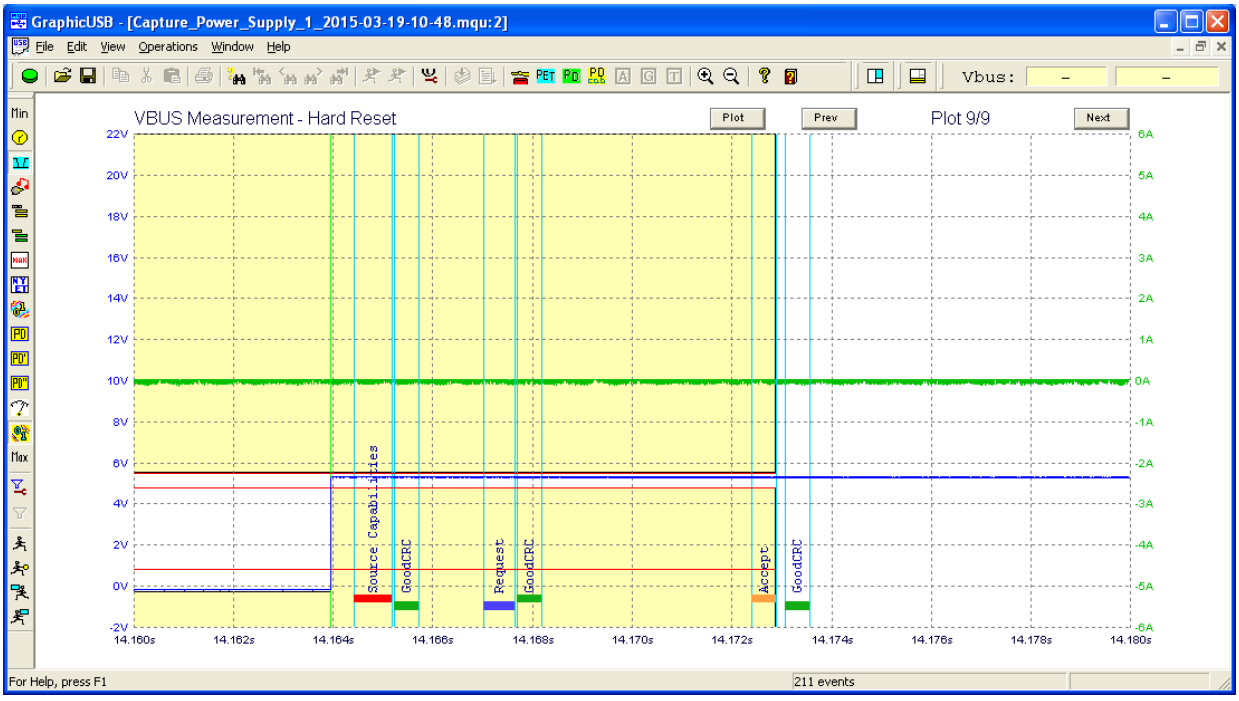


Hard Reset

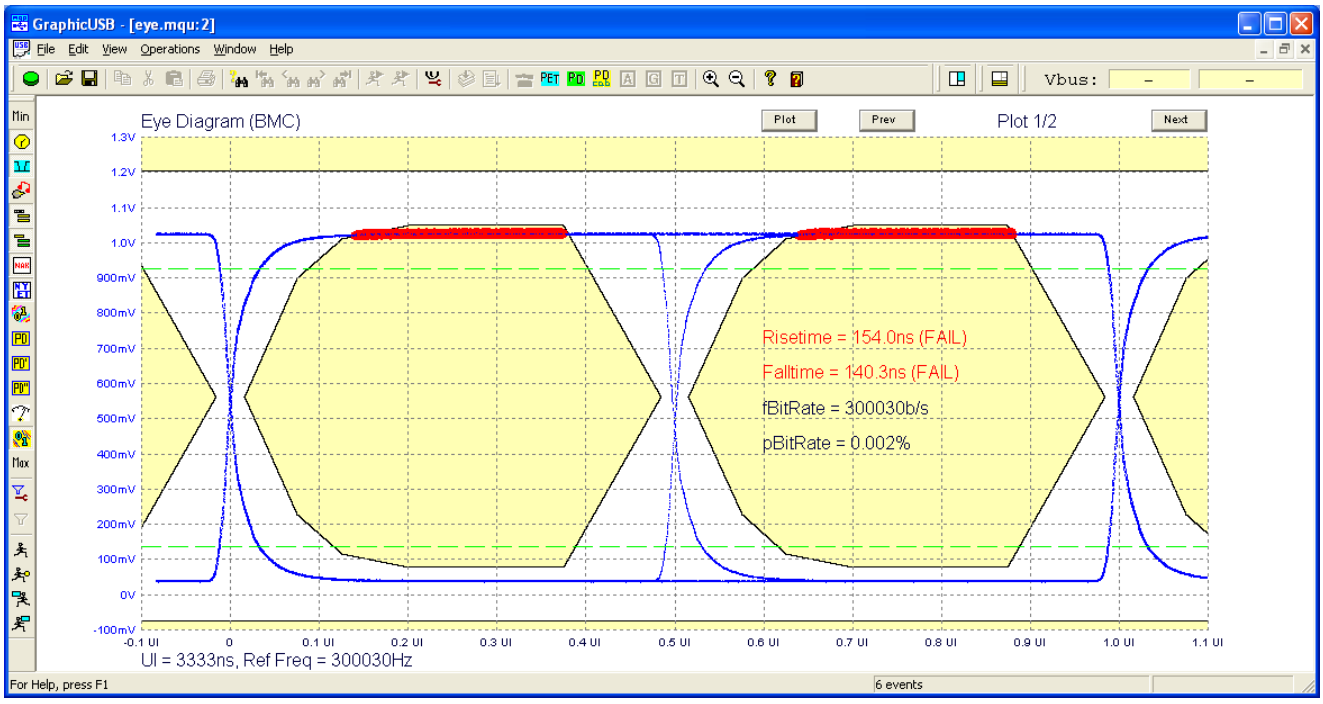
Another example is this Compliance Test capture of a Hard Reset, the VBUS voltage and current waveforms are plotted against the appropriate mask, defined by the PD Specification. The blue vertical lines show the boundaries of the PD messages (described in more detail on zooming in). The waveforms will be coloured red if they intersect the mask.



Zooming in on the end of this capture (shown below) we see the exact timing and description of the PD messages, in relation to the VBUS waveforms



Eye Diagram



One important capability of the Tester is to run an Eye Diagram test as specified in the CTS Compliance Test.

The accuracy of this capture is not degraded by external connections, or potential incorrect settings of external third party oscilloscopes as with other solutions.

The Tester will establish PD communication with the UUT, transmit a BIST Mode 2 request, and during the 30-60ms continuous transmission resulting, will capture samples of the waveform from the UUT.

The UUT may be a PD device or an electrically marked Type-C cable.

The samples are plotted against the CTS Test Specification defined mask, with an indication of any places where the mask is intersected.

The other specification parameters; Risetime, Falltime, BitRate, and Bitrate drift are also calculated and displayed (and displayed in red if out of spec).

The original captured signal, used to build the eye diagram, is also available for display

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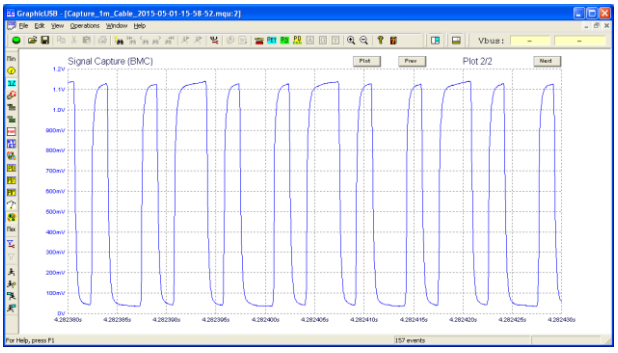
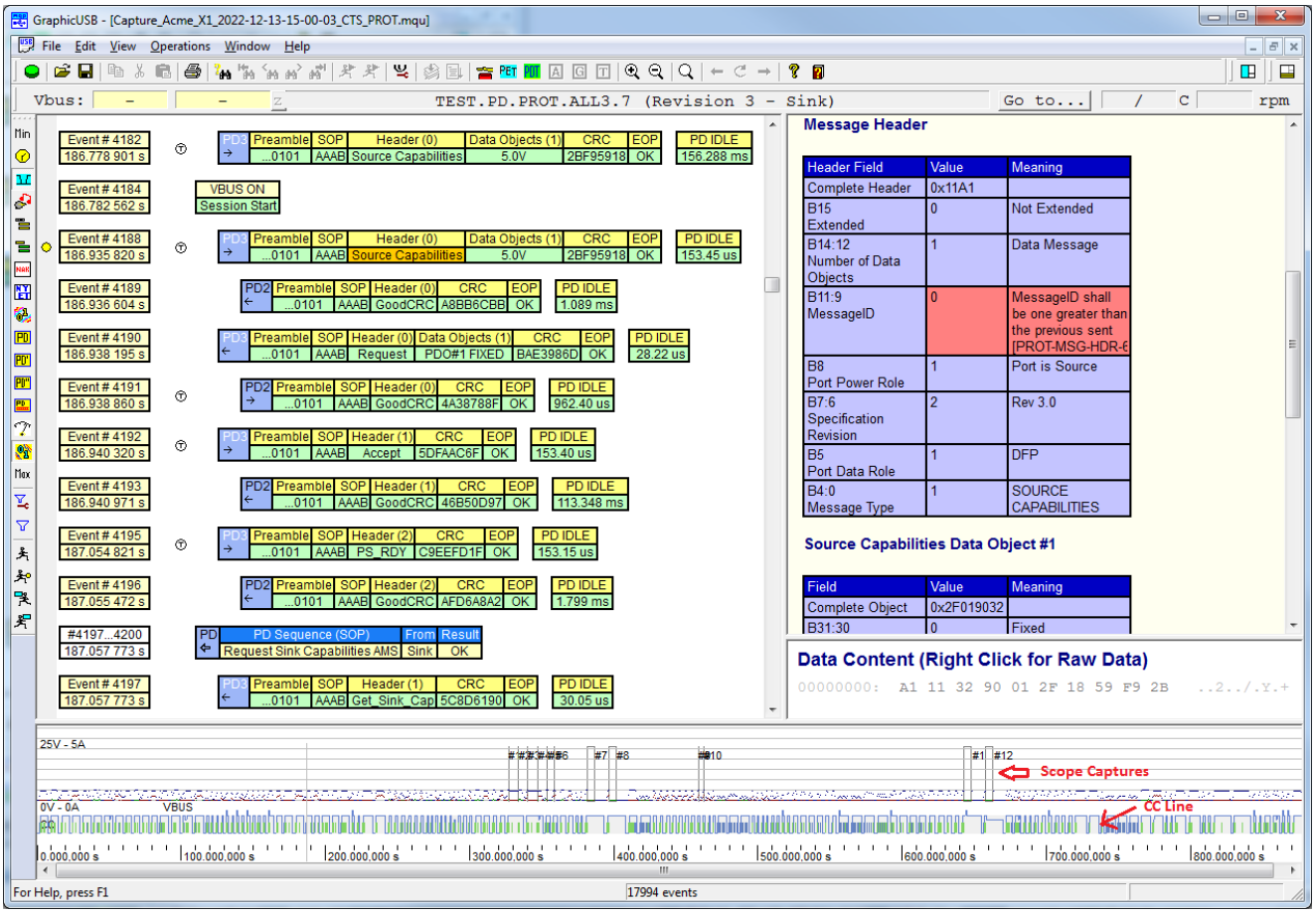


GraphicUSB Application

The Packet-Master product is supplied complete with our GraphicUSB software application.



The GraphicUSB Capture File View

Event Capture Pane

This pane (on the left) displays the captured events, either in summary header form, or detailing every event which is captured. Any event may then be selected for complete analysis.

Colour is used to draw attention to any specification violations.

Detail Pane

This displays the detailed analysis, down to bit level, of the event selected.

Detailed analysis of any specification violations is available in this panel.

Data Pane

This is found below the Detail Pane. It shows the decoded data found in the current event. The raw undecoded data may also be viewed.

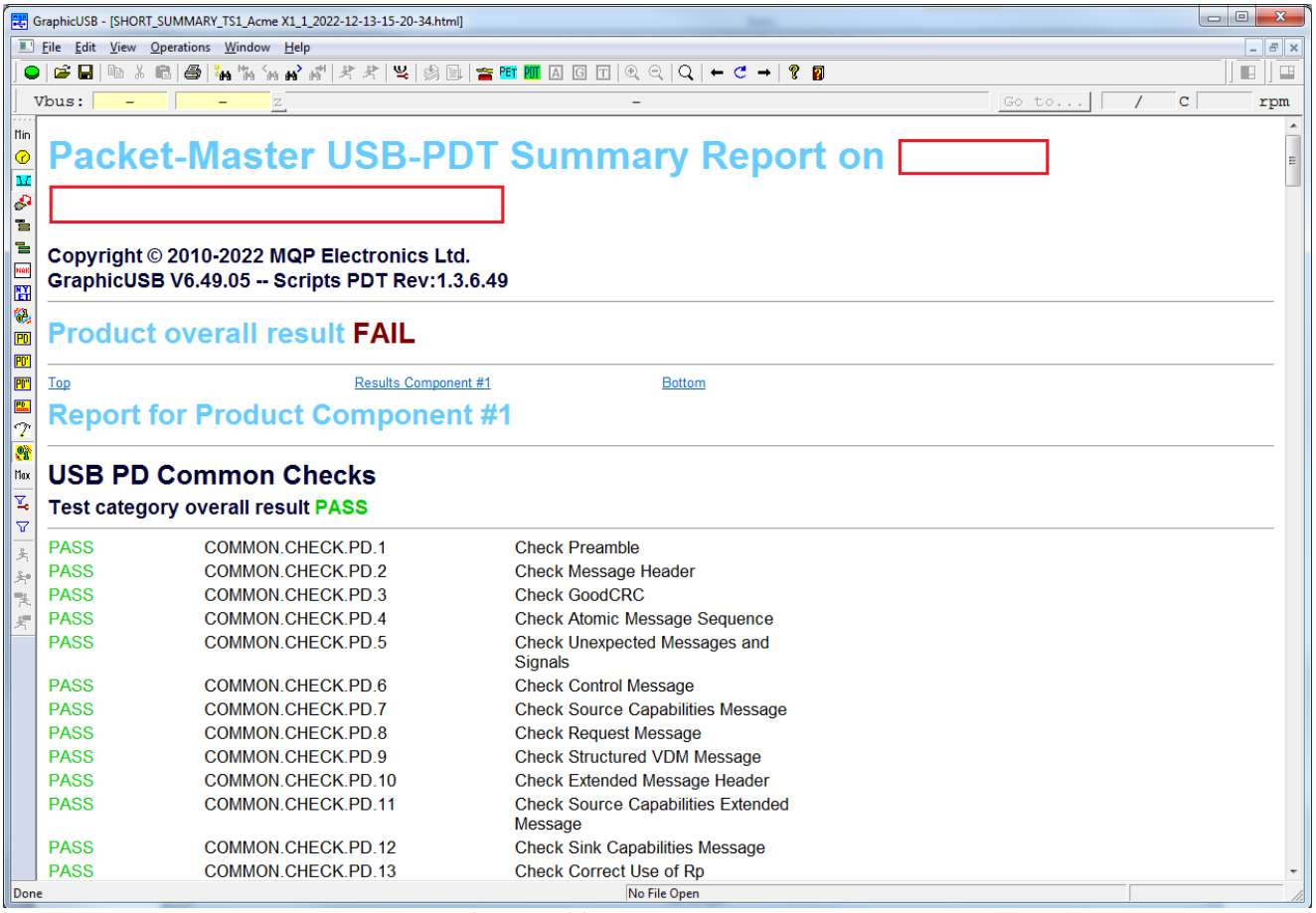
Timeline Panel VBUS Voltage and Current Frames Events

In the zoomable panel along the bottom is a VBUS voltage and current display, lasting for the full duration of the capture.

Below the voltage and current waveforms is a graphical representation of the CC Line state. It shows the Rd/Rp connection state and the position in time of each PD packet. Hovering over any of these shows a tooltip describing the packet.

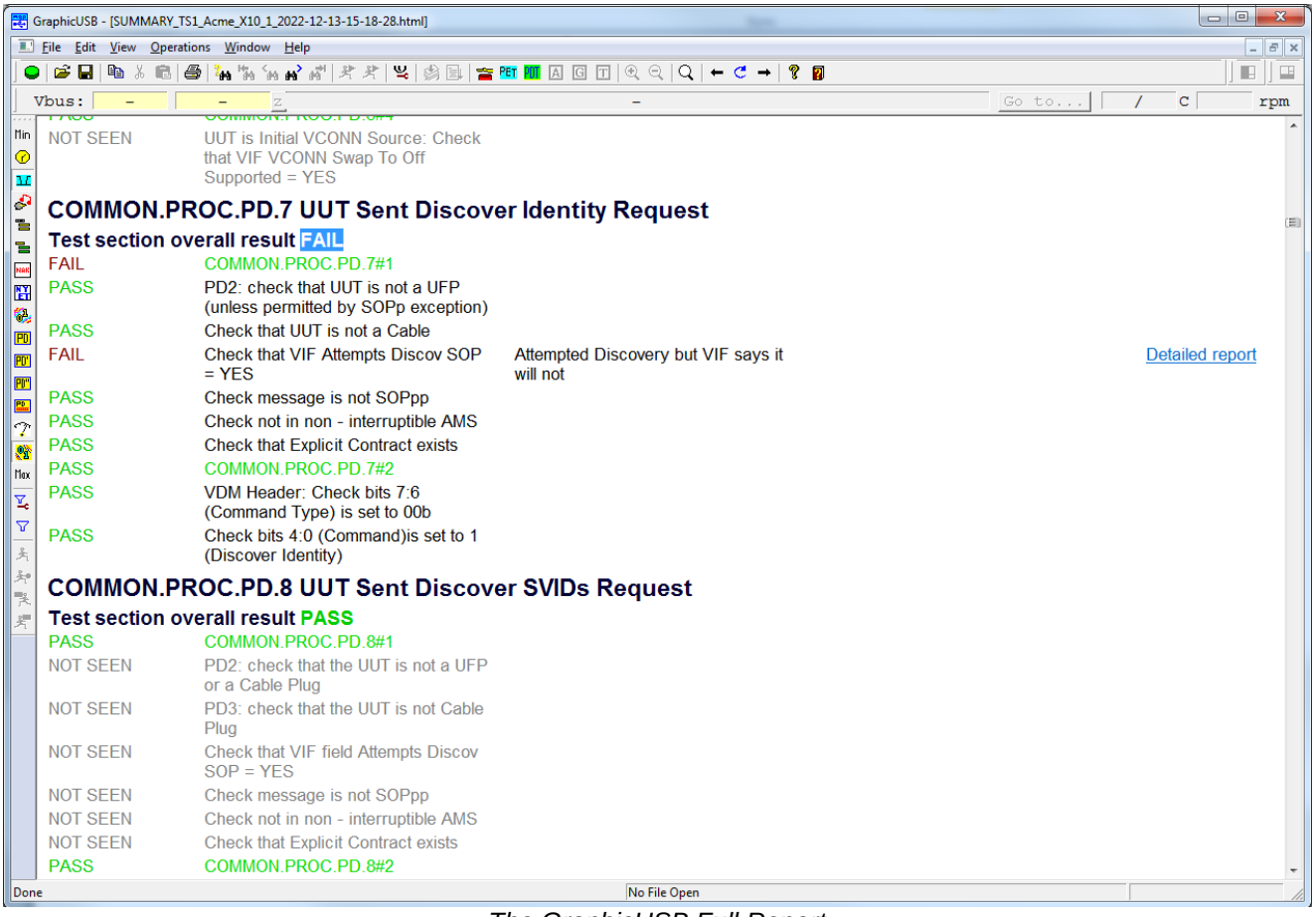
Together these displays allow the developer to confirm the timing relationship between messages and voltage/current transitions.

Report Views



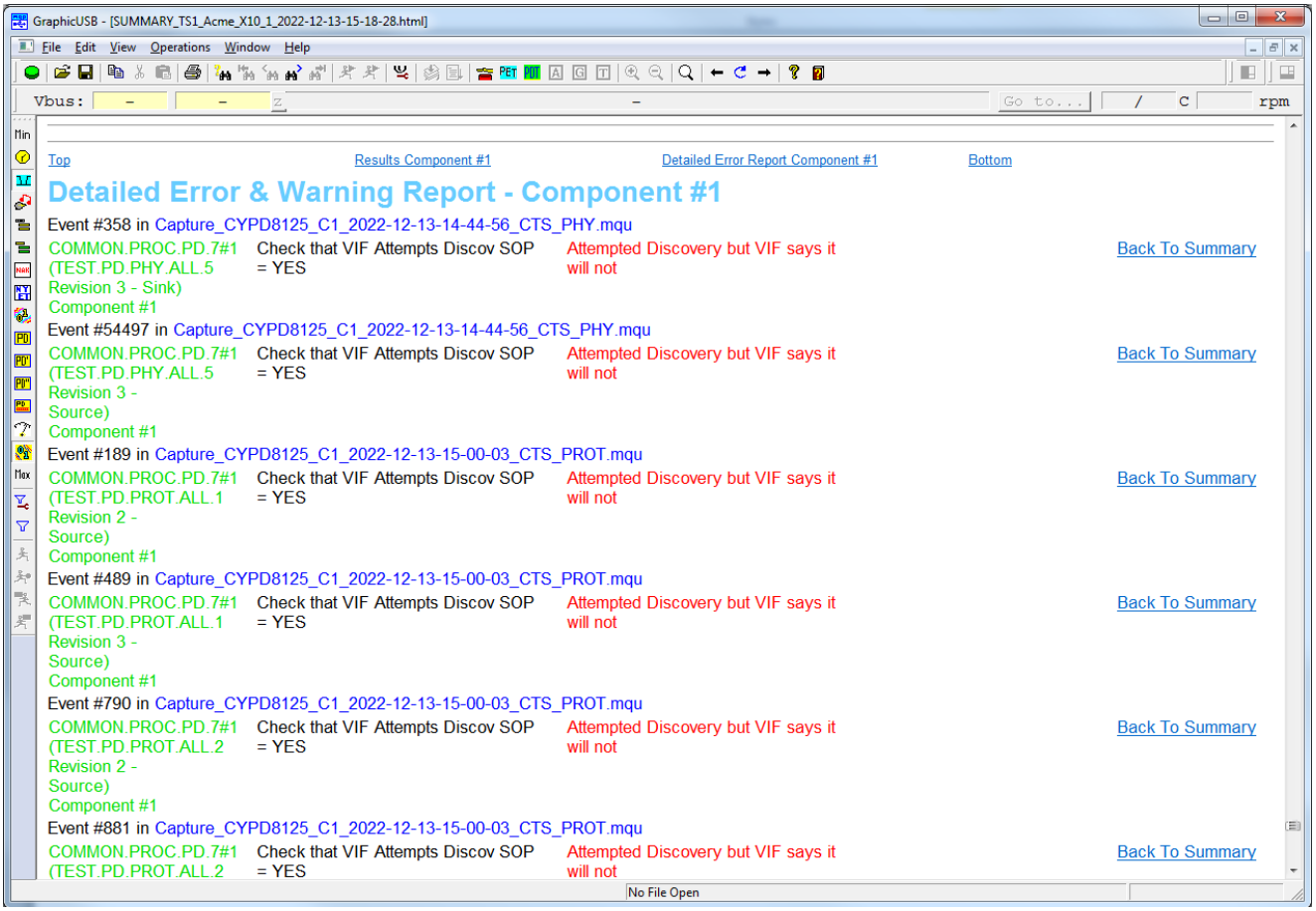
The GraphicUSB Summary Report

The Summary Report shows the results of the top level checks, to assist in a quick evaluation of the product test.



The GraphicUSB Full Report

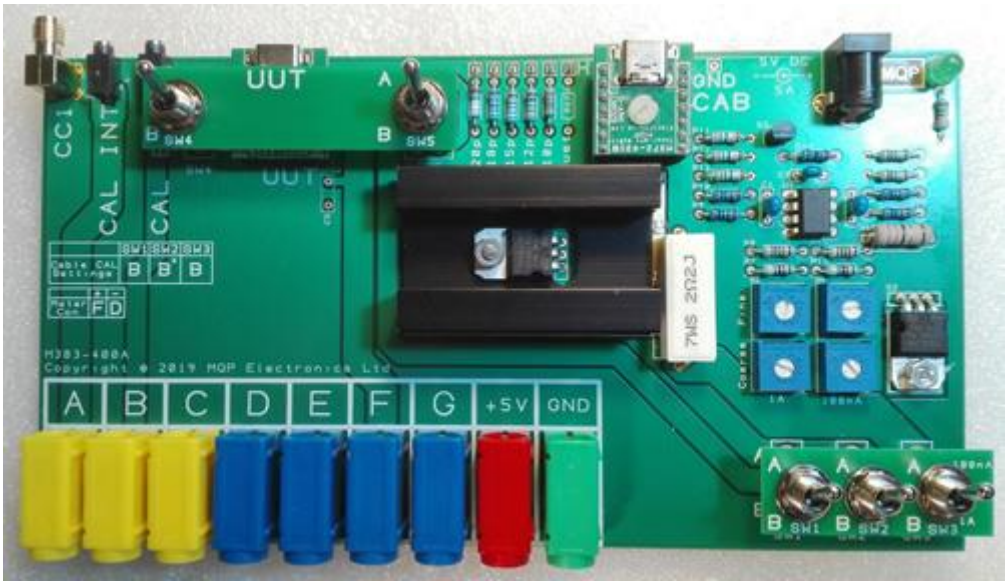
The Full Report shows the results of the low level checks, to allow the user to locate the actual issue being failed. Clicking on Detailed Report will reveal a description of where this error (or these errors) occurred during the tests.



The GraphicUSB Error Details

The Error Details allow the user to locate the actual Event # in the capture file where the error occurred.

Optional System Extra – Calibration Jig



To avoid the need for international shipping to calibrate the Packet-Master PDT-EPR, we have developed a user-based calibration kit. The user has only to provide a suitable currently calibrated multimeter, for example the Keysight U1241B.

The unit is supplied in a protective carrying case, with its own power supply, a suitable mains cable, and two test cables.

Optional System Extra – Analyser POD

The USB-PDT Analyser Pod is an option for the Packet-Master PDT-EPR to allow it to be used as a non-intrusive Analyser for PD-Communication between two third-party PD devices. It is equally suitable for devices connected by a separate PD cable, or for the case where one of the devices has a captive cable.

Optional System Extra – FRS Switch AC-DC

For testing UUTs with FRS capability it is necessary to be able to interrupt the AC supply to the Initial Source under test, and also in some cases the DC cable in the UUT Setup. Our combined FRS-AC-DC Switch is designed to make such testing as uncomplicated as possible. The picture below shows the unit arrangement.

Physical Parameters

PDT-EPR (Tester)	
Size:	250 x 180 x 75 mm
Weight:	2040 gm (including BT3 Plug-in module) 725 gm for PSU
Temperature:	0°C - 40°C
Humidity:	20% - 80% non condensing
USB Current draw	Zero mA from USB.
Using the external power supply 24V/13.75A (included) is the required mode of operation.	

PDT-EPR v USB-PDT Comparison Chart

Feature	**USB-PDT**	**PDT-EPR**
VBUS Generator	3V - 21V, 5A	3V - 48V, 5A
VBUS Settable Current Limit	No	1A – 5A
Current Sink	0 – 5A 100W	0 – 5A 240W
Protocol	SPR Only	EPR and SPR
Voltage Measurement Range	0V to 21V	0V – 55V
Cooling Arrangements	100W Capable	240W Capable
Test Cable	Custom 20V/5A Cable	Custom 50V/5A Cable
External Power Supply Provided	24V/8.3A	24V/13.75A

Product Coding

Designation	Description	Included with PDT-EPR	Availability
PDT-EPR	PDT-EPR base unit with permanent registration of CTS software	✓	Current
PDT-EPR-PSU	External power supply unit for PDT-EPR	✓	Current
PDT-BT3	Plug-in with Type-C receptacle.	✓	Current
MQP-CAB-EPR	Calibrated Test Cable	✓	Current
FRS-AC-DC	Switch box for FRS AC and DC testing.	Available separately	Current
ANA-POD	Analyser POD. Add-on that captures interaction between two external PD devices.	Available separately	Current
BT3-CAL	Calibration jig. Allows user to perform annual calibration on the PDT-EPR, using their own calibrated multimeter.	Available separately	Current

Coding for Upgrade Paths

Designation	Description
PDT-EPR-UPGD-CTS	Upgrade of existing USB-PDT to support EPR, including permanent registration of CTS software. Does not include BT3
PDT-EPR-UPGD	Upgrade of existing USB-PDT to support EPR, for customers who already have permanent registration of CTS software. Does not include BT3

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